ABSTRACT OF THE DISCLOSURE

A semiconductor memory device includes memory cells, a memory cell array, word lines, select gate lines, first and second row decoders, and a control circuit. The memory cell includes a first MOS transistor with a stacked gate formed on a first well region and a second MOS transistor having a drain connected to a source of the first MOS transistor. The word line connects in common control gates of the first MOS transistors. The select gate line connects in common gates of the second MOS transistors. The first row decoder in a write operation, applies a positive and negative potentials to the selected word line and the first well region, respectively and after the write operation, brings the selected word line and the first well region into a floating state. The control circuit short-circuits the selected word line and first well region in the floating state.